IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No.	:	6,950,903
Issued	:	September 27, 2005
Application No.	:	09/892,566
Applicant	:	SOLOMON *et al.*
For	:	Power Reduction for Processor Front-End By Caching Decoded Instructions
Docket No.	:	02207/10607
Customer No.	:	23838

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER 37 C.F.R. § 1.181(a)
REQUESTING RE-PUBLICATION OF PATENT

Sir:

Under the authority afforded the Director under 35 U.S.C. §§ 10 and 254, Patentee petitions for republication of U.S. Patent 6,950,903 B2, issued September 27, 2005, due to extensive errors which are the mistake of the USPTO. A copy of U.S. Patent 6,950,903 B2 is attached hereto as Appendix "A".

Upon proofreading the patent, Patentee learned on July 11, 2006 that the claims published on the face of the patent are not the claims as amended in Applicants' final amendment dated April 14, 2005, and allowed with an Examiner's Amendment in the Notice of Allowance dated May 25, 2005 (claims 1-6, 10-15 and 27-41). Although twenty-seven claims were allowed, only 12 claims were published – all 12 of which are incorrect. The claims as published appear to be a subset of the claims from a prior-filed Response to Office Action, dated May 10, 2004.

A Certificate of Correction under 35 U.S.C. § 254 is attached herewith (Appendix "B"), presenting allowed claims 1-6, 10-15, and 27-41, renumbered as 1-27. A copy of the claims as allowed and originally numbered, including the Examiner's Amendment, is also attached (Appendix "C"). In view of the extent of the changes to the Patent, Patentee respectfully

requests that the Director issue a corrected patent without charge in lieu of and with like effect of the attached Certificate of Correction, as expressly permitted in 35 U.S.C. § 254.

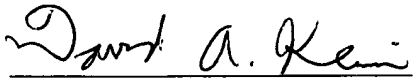
Should the Director conclude that the Office issuing a patent with the wrong claims does not warrant republication, Patentee respectfully requests that the Director instead issue the attached Certificate of Correction under 35 U.S.C. § 254, replacing all claims in the Patent.

Patentee also attaches a Certificate of Correction under 35 U.S.C. § 255 (Appendix "D"), and **authorizes deduction of the $100.00 required under 37 C.F.R. § 1.20(a) from Deposit Account No. 11-0600.** A minor grammatical error went unnoticed in allowed claim 10, and an error in claim 15 was inadvertently overlooked during prosecution of the application as well. Specifically, the preambles of claims 10-14 were replaced in the Amendment filed November 22, 2004, but mistakenly, an "a" was not changed to "an" in claim 10, and the new preamble was not otherwise carried forward into claim 15, which also depends from independent claim 10. As claims 10 and 15 are renumbered as claim 7 and 12, respectively on the Certificate of Correction under § 254, the claims are also renumbered as claim 7 and 12 in the attached Certificate of Correction under § 255. Patentee submits that the changes to the claims on the attached sheet are to correct typographical mistakes made in good faith, do not constitute new matter, and do not require reexamination. The existence of the mistakes and the appropriate corrections are readily apparent on the face of the claims.

If the Office republishes U.S. Patent 6,950,903 B2, Patentee asks that the Certificate of Correction under § 255 either be attached to the republication, or at the Director's discretion, be integrated into the republished claims. Otherwise, please issue the Certificate of Correction under 35 U.S.C. § 255 as an addendum to the Certificate of Correction under 35 U.S.C. § 254.

Patentee authorizes the Commissioner to charge any fees determined to be due and to credit any overpayment to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON LLP



David A. Klein
Reg. No. 46,835

Dated: August 3, 2006

Kenyon & Kenyon LLP
1500 K Street, N.W., Suite 700
Washington, D.C. 20005
Tel: (202) 220-4200
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APPENDIX A

U.S. Patent 6,950,903 B2

APPENDIX B

Certificate of Correction under 35 U.S.C. § 254

PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,950,903

APPLICATION NO. : 09/892,566

ISSUE DATE : September 27, 2005

INVENTOR(S) : SOLOMON et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

7. ~~A~~ An apparatus, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to unpower the data fetch unit selectively.

12. The ~~front-end processing system~~ apparatus of claim 11, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processing system.

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APPENDIX C

Claims numbered as allowed by Examiner

Listing of claims:

1. A processor, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

an instruction processing system coupled to the instruction cache, having a power control input coupled to the hit/miss output of the UOP cache.

2. The processor of claim 1, wherein the instruction cache comprises a cache lookup unit and a cache fetch unit, the cache fetch unit having a power control input coupled to the hit/miss output of the UOP cache.

3. The processor of claim 1, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the power control input.

4. The processor of claim 1, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss output.

5. The processor of claim 4, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit.

6. The processor of claim 5, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

7.-9. (Canceled)

10. A apparatus, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to unpower the data fetch unit selectively.

11. The apparatus of claim 10, further comprising an instruction processing system in communication with the instruction cache, the hit/miss indicator to unpower the instruction processing system selectively.

12. The apparatus of claim 11, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

13. The apparatus of claim 10, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss indicator.

14. The apparatus of claim 13, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

15. The front-end processing system of claim 14, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processing system.

16.-26. (Canceled)

27. A method, comprising:

providing an address in parallel to a micro-instruction cache and to an instruction processing system;

if the address hits the instruction processing system, then, within the instruction processing system:

outputting addressed data from an instruction cache performing instruction synchronization of the output data, and

decoding instructions obtained therefrom to obtain decoded micro-instructions; and

if the address hits the micro-instruction cache, then:

outputting addressed micro-instructions from the micro-instruction cache, and

terminating performance of the outputting and the decoding operations of the instruction processing system, if any, that result from the providing of the address to the instruction processing system.

28. The method of claim 27, wherein the terminating further comprises withholding clock signals from the instruction processing system.

29. The method of claim 27, wherein the terminating further comprises generating a disabling output signal from the micro-instruction cache to the instruction cache.

30. The method of claim 27, further comprising delaying outputting the addressed micro-instructions from the micro-instruction cache by an amount representing a difference between processing time of the instruction processing system and processing time of the micro-instruction cache.

31. A method, comprising:

applying an address in parallel to first and second caches, the caches storing data in mutually different formats,

if the address hits the second cache, then:

outputting addressed data from the second cache, and

converting the output data to a format of the first cache;

if the address hits the first cache, then:

outputting addressed data therefrom, and

terminating performance of the outputting and the converting operations of the second cache, if any, that result from the applying of the address to the second cache.

32. The method of claim 31, wherein the terminating further comprises withholding clock signals from the second cache.

33. The method of claim 31, wherein the terminating further comprises generating a disabling output signal from the first cache to the second cache.

34. The method of claim 31, further comprising delaying outputting the addressed data from the first cache by an amount representing a difference between processing time of the second cache and processing time of the first cache.

35. A system, comprising:

a processor for performing instruction pre-processing and to output decoded instructions, the processor comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

the instruction cache having a first cache lookup unit and a data fetch unit, and

the hit/miss indicator to selectively disable operation of the data fetch unit, and

an execution unit to receive and execute the decoded instructions from the processor.

36. The system of claim 35, further comprising a memory to store and retrieve data associated with the decoded instructions.

37. The system of claim 35, further comprising an instruction processor in communication with the instruction cache, the hit/miss indicator to unpower the instruction processor selectively.

38. The system of claim 37, wherein the instruction processor comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

39. The system of claim 35, wherein the UOP cache comprises a second cache lookup unit and a cache fetch unit, the second cache lookup unit coupled to the hit/miss indicator.

40. The system of claim 39, wherein the UOP cache further comprises a delay element provided between the second cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

41. The system of claim 40, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processor.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with David A Klein on May 19, 2005.

The application has been amended as follows:

In the claims:

In claim 35 at line 7 after "disable" insert "operation of".

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

May 23, 2005

APPENDIX D

Certificate of Correction under 35 U.S.C. § 255

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,950,903

APPLICATION NO. : 09/892,566

ISSUE DATE : September 27, 2005

INVENTOR(S) : SOLOMON *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

1. A processor, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

an instruction processing system coupled to the instruction cache, having a power control input coupled to the hit/miss output of the UOP cache.

2. The processor of claim 1, wherein the instruction cache comprises a cache lookup unit and a cache fetch unit, the cache fetch unit having a power control input coupled to the hit/miss output of the UOP cache.

3. The processor of claim 1, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the power control input.

4. The processor of claim 1, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss output.

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5. The processor of claim 4, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit.

6. The processor of claim 5, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

7. A apparatus, comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to unpower the data fetch unit selectively.

8. The apparatus of claim 7, further comprising an instruction processing system in communication with the instruction cache, the hit/miss indicator to unpower the instruction processing system selectively.

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected s shown below:

9. The apparatus of claim 8, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

10. The apparatus of claim 7, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss indicator.

11. The apparatus of claim 10, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

12. The front-end processing system of claim 11, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processing system.

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

13. A method, comprising:

providing an address in parallel to a micro-instruction cache and to an instruction processing system;

if the address hits the instruction processing system, then, within the instruction processing system:

outputting addressed data from an instruction cache performing instruction synchronization of the output data, and

decoding instructions obtained therefrom to obtain decoded micro-instructions; and

if the address hits the micro-instruction cache, then:

outputting addressed micro-instructions from the micro-instruction cache, and

terminating performance of the outputting and the decoding operations of the instruction processing system, if any, that result from the providing of the address to the instruction processing system.

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

14. The method of claim 13, wherein the terminating further comprises withholding clock signals from the instruction processing system.

15. The method of claim 13, wherein the terminating further comprises generating a disabling output signal from the micro-instruction cache to the instruction cache.

16. The method of claim 13, further comprising delaying outputting the addressed micro-instructions from the micro-instruction cache by an amount representing a difference between processing time of the instruction processing system and processing time of the micro-instruction cache.

17. A method, comprising:

applying an address in parallel to first and second caches, the caches storing data in mutually different formats,

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INVENTOR(S) : SOLOMON *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

if the address hits the second cache, then:

outputting addressed data from the second cache, and

converting the output data to a format of the first cache;

if the address hits the first cache, then:

outputting addressed data therefrom, and

terminating performance of the outputting and the converting operations of the second cache, if any, that result from the applying of the address to the second cache.

18. The method of claim 17, wherein the terminating further comprises withholding clock signals from the second cache.

19. The method of claim 17, wherein the terminating further comprises generating a disabling output signal from the first cache to the second cache.

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INVENTOR(S) : SOLOMON *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

20. The method of claim 17, further comprising delaying outputting the addressed data from the first cache by an amount representing a difference between processing time of the second cache and processing time of the first cache.

21. A system, comprising:

a processor for performing instruction pre-processing and to output decoded instructions, the processor comprising:

a micro-operation (UOP) cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

the instruction cache having a first cache lookup unit and a data fetch unit, and

the hit/miss indicator to selectively disable operation of the data fetch unit, and

an execution unit to receive and execute the decoded instructions from the processor.

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INVENTOR(S) : SOLOMON *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

22. The system of claim 21, further comprising a memory to store and retrieve data associated with the decoded instructions.

23. The system of claim 21, further comprising an instruction processor in communication with the instruction cache, the hit/miss indicator to unpower the instruction processor selectively.

24. The system of claim 23, wherein the instruction processor comprises an instruction synchronizer and an instruction decoder coupled to the hit/miss indicator.

25. The system of claim 21, wherein the UOP cache comprises a second cache lookup unit and a cache fetch unit, the second cache lookup unit coupled to the hit/miss indicator.

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

26. The system of claim 25, wherein the UOP cache further comprises a delay element provided between the second cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

27. The system of claim 26, wherein the delay element is characterized by a delay corresponding to a processing time of the instruction processor.

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